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TWO STAGE OP-AMP USING CMOS–AREVIEW

Mr. Bhushan Bangadkar
PG Scholar
Electronics and Communication Engineering,
G H Raisoni Academy of Engineering and Technology,
Nagpur, Maharashtra, India

Mr. Amit Lamba
Assistant Professor
Electronics and Communication Engineering,
G H Raisoni Academy of Engineering and Technology,
Nagpur, Maharashtra, India

Mr. Vipin Bhure
Assistant Professor
Electronics and Communication Engineering,
G H Raisoni Academy of Engineering and Technology,
Nagpur, Maharashtra, India

Abstract— Operational Amplifier (op-amp) is a basic building block of many analog and mixed signal systems. Many different types of op-amp are used to achieve various functions, such as DC biasing, high speed amplifying, reduced voltage supply, high gain. To achieve these parameter successfully there are several techniques.The op-amp contains two stages to increase gain and improve slew rate, voltage swing, phase margin. In high resolution low voltage application where Thermal Noise and Op-amp output Swing are important then two stage op-amp is preferable to single stage. In circuits the gain provided by the input stage is not sufficient, so there is an additional amplification is required which is provided by second stage.

Keywords—Two stage Op-amp, CMO, Amplification.

I. INTRODUCTION

Operational amplifier (op-amp) is the most versatile and an integral part of much analog and mixed-signal system. They are employed from dc bias application to high speed amplifier and filters. General purpose op-amp can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, and many other applications. Its performance makes significant impact on the analog system. Nowadays, due to the industry trend of applying standard process technologies to implement both analog circuits on the same chip, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design in a mixed-signal system.

The implementation of CMOS op-amp that combines a considerable dc gain with higher unity gain frequency has been a most difficult problem. There have been several circuits proposed to evaluate this problem. The purpose of the design methodology in this project is to propose accurate equations for the design of high-gain two stage CMOS op-amp. In some application the gain and/or output swing provided by cascode op-amp are not adequate. In such cases, we resort to two stage op-amp, with the first stage providing a high gain and the second large swing. The application in which high gain low power op-amp with flexible noise performance used are as in medical field , active filters and signal processing, in sensors applications.

1.1 Block Diagram of Two Stage Op-amp

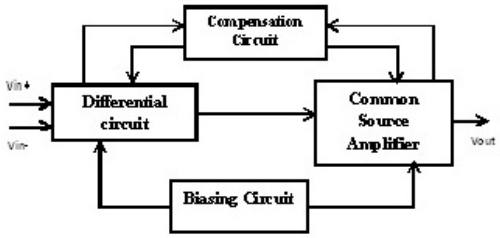

Fig 1: Block diagram of two stage op-amp

For much analog circuit design, operational amplifier is important block. The accuracy and speed of these circuits depends on bandwidth and DC gain of the op-amp. As larger bandwidth and gain, speed and accuracy of amplifier also larger. The simplified block diagram is shown in figure1. Differential amplifier is the first block of circuit which has two input inverting and non-inverting voltage. It gives differential current or differential voltage at output which depends on differential input voltage. The gain provided by input is not sufficient so there is additional amplification is necessary which is provided by common source second stage, driven by differential gain stage output. The common source second stage increases the DC gain for an given voltage supply by an order of magnitude and increases the output signal swing. The biasing circuit is used to provide proper operating point to each transistor in its saturation region. Output Buffer stage provides the low impedance at output and larger the output current needed to drive the load of op-amp of it used to improve the slew rate. Manyapplications do not need low output impedance

hence output stage can be dropped. Output buffer is not required if the op-amp is intended to drive a small purely capacitive load. The circuit is used as an operational transconductance amplifier when the output stage is not used.

1.2 Circuit Operations

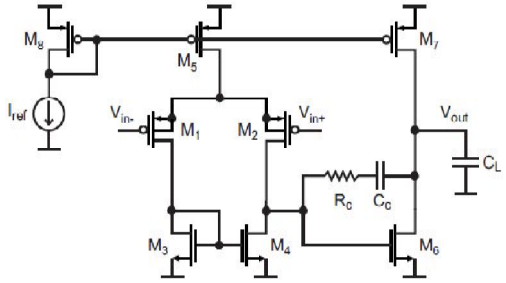

Fig 2 : Circuit diagram of two stage op-amp

The figure shows the topology of standard CMOS op-amp which is made up of three sub parts,they are as differential gain stage, second gain stage and biasing network.

1.3 Differential Gain Stage

Transistors M1,M2,M3 and M4 cosntitute the first stage of op-amp which is diffrential amplifier. The gate of M1 is non inverting input and gate of M2 is inverting input.The gain of this stage is the tranconductance of M1 times the total output esistanceseen at the drain of M2.The current mirror used in in this circuit has three distinct advantages. Frist in small amount of cip area the use of active load devices creats a large output resistance. Current mirror topology performs the diffrential to single ended conversionof the input signal.and the load helps with the comman mode rejection ratio. By using M3 and M4 (current mirror) conversion from diffrential to single ended is achieved. M3 and M4 mirror the current from M1and subtracted from M2.The diffrential current from M1 and M2 multiplied bythe output resistance of input stage which gives single ended output voltage which is part input to the next stage.

1.4 Common Source Second Gain Stage

Current sink inverter is the second stage. To provide additional gain second gain stage is used which is of transistor M6 and M7. The output receives from drain of M2 and amplifies it through M6 by common source configurations.

1.5 Biasing circuit

By using four transistors biasing of op-amp is achieved.Transistors M8 and M9 form a simple current mirror bias string that supplies a voltage between the gate and source ofM7 and M6. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. Proper biasing of the other transistors in the circuit (M1-M5) is controlled by the node voltages present in the circuit itself.

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II. LITERATURE REVIEW

The designing of high performance analog integrated circuits is becoming most essential with the continuous trend toward the reduced supply voltage and transistor channel length. MOS is the most success among all because it can be scaled down to smaller dimensions for higher performance. The size can be reduced to micrometer or nanometres for getting higher performance.

2.1 "High Performance Full-Differential Op-Amp Design"

This paper based on telescope structure where 0.18µm CMOS technology is used with 3.3V power supply and simulation is done using cadence tool. In this design to meet the basic specification of high-performance op-amps two stage structure is used. Two stage amplifiers contain zero poles, which harm the stability of amplifiers. To make amplifiers stable, miller compensation are used to compensate the zero poles.

Telescopic structure used in this design is high-speed because it has lower parasitic capacitor in the secondary pole. The design uses a sleeve-type structure of the circuit in first stage, and common source amplifier in the second stage, so that the circuit has a higher gain in the second grade and is able to achieve higher output swing. After simulation the AC characteristics, obtained gain is 129.4dB, Gain bandwidth is 101.7m, Phase margin is 53.64 degree. Slew rate is 32V/us.[1]

2.2 "A New Two Stage Op-Amp Using Gate Driven and Positive Feedback Techniques"

In this paper two stage op-amp is designed using gate driven and positive feedback techniques using 0.18um CMOS technology with 1.2V supply voltage while power dissipation is approximately unchanged, the DC gain of conventional two stage op-amp is increase about 20dB but no significant change will be made in unity gain bandwidth of the circuits. In order to increase the DC gain, the positive feedback structure can also be utilized. However this technique can make the architecture unstable.

A two stage op-amp is chosen in which a folded cascade OTA is chosen in the first stage and to have high output swing a common source structure is chosen for the second stage. Besides, a hybrid-cascode compensation method is used for

compensation of the frequency response. The simulation result shows a DC gain of 95dB, unity gain frequency of 540MHZand phase margin of 65 degree. The slew rate is 200V/us and op-amp dissipates about 2.45mW.[2]

2.3 "Designing 1-V Op Amps Using Standard Digital CMOS Technology"

This paper focuses on developing analog circuit techniquesthat are compatible with future CMOS technologies. Note thatcircuit techniques which permit low voltage operation withlarge thresholds offer the potential for more thoroughly utilizingthe technology at any voltage range even if low thresholdvoltage technologies become standard.

Design techniques for facilitating 1-V operation are discussed and 1-V analogbuilding block circuits are presented. Most of these circuitsuse the bulk-driving technique to circumvent the metal–oxide–semiconductor field-effect transistor turn-on (threshold)voltage requirement. Finally, techniques are combined within a1-V CMOS operational amplifier with rail-to-rail input andoutput ranges. While consuming 300 µW, the 1-V rail-to-railCMOS op amp achieves 1.3-MHz unity-gain frequency and 57 phase margin for a 22-pF load capacitance. [3]

III. CONCLUSION

From the above related paper, we come to the conclusion that for high performance op-amp telescopic structure is used and achieved good performance in gain, bandwidth and phase margin. It also improved by gate driven and positive feedback techniques. Some of the 1V capable analog circuit building blocks described in the paper were used to design a 1V CMOS op-amp with rail-to-rail ICMR and output swing.

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